# Power MOSFET 75 Amps, 30 Volts

# N-Channel TO-220 and D<sup>2</sup>PAK

This Logic Level Vertical Power MOSFET is a general purpose part that provides the "best of design" available today in a low cost power package. Avalanche energy issues make this part an ideal design in. The drain—to—source diode has a ideal fast but soft recovery.

#### **Features**

- Ultra-Low R<sub>DS(on)</sub>, Single Base, Advanced Technology
- SPICE Parameters Available
- Diode is Characterized for Use in Bridge Circuits
- I<sub>DSS</sub> and V<sub>DS(on)</sub> Specified at Elevated Temperatures
- High Avalanche Energy Specified
- ESD JEDAC Rated HBM Class 1, MM Class B, CDM Class 0
- Pb-Free Packages are Available

#### **Typical Applications**

- Power Supplies
- Inductive Loads
- PWM Motor Controls
- Replaces MTP75N03HDL and MTB75N03HDL in Many Applications

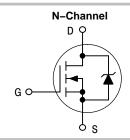


#### ON Semiconductor®

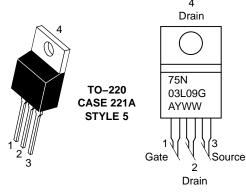
http://onsemi.com

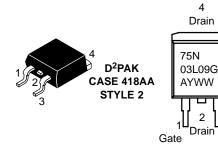
#### 75 AMPERES, 30 VOLTS

 $R_{DS(on)} = 8 \text{ m}\Omega$ 



# MARKING DIAGRAMS & PIN ASSIGNMENTS





75N03L09 = Device Code A = Assembly Location

 $egin{array}{lll} Y &=& Year \\ WW &=& Work Week \\ G &=& Pb-Free Package \\ \end{array}$ 

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Source

#### **MAXIMUM RATINGS** ( $T_J = 25^{\circ}C$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	30	Vdc
Drain-to-Gate Voltage (RGS = $10 \text{ M}\Omega$ )	$V_{DGB}$	30	Vdc
Gate-to-Source Voltage - Continuous	$V_{GS}$	±20	Vdc
Non–repetitive (tp ≤ 10 ms)	$V_{GS}$	±24	Vdc
Drain Current  - Continuous @ $T_C = 25^{\circ}C$ - Continuous @ $T_C = 100^{\circ}C$ - Single Pulse (tp $\leq 10 \mu s$ )	I <sub>D</sub> I <sub>D</sub> I <sub>DM</sub>	75 59 225	Adc Apk
Total Power Dissipation @ T <sub>C</sub> = 25°C  Derate above 25°C  Total Power Dissipation @ T <sub>A</sub> = 25°C (Note 1)	P <sub>D</sub>	125 1.0 2.5	W W/°C W
Operating and Storage Temperature Range	T <sub>J</sub> and T <sub>stg</sub>	-55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^{\circ}C$ ( $V_{DD} = 38$ Vdc, $V_{GS} = 10$ Vdc, $L = 1$ mH, $I_L(pk) = 55$ A, $V_{DS} = 40$ Vdc)	E <sub>AS</sub>	1500	mJ
Thermal Resistance  - Junction-to-Case  - Junction-to-Ambient  - Junction-to-Ambient (Note 1)	$egin{array}{c} R_{ heta JC} \ R_{ heta JA} \ R_{ heta JA} \end{array}$	1.0 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	TL	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using the minimum recommended pad size.

### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>	
NTP75N03L09	TO-220	50 Units/Rail	
NTP75N03L09G	TO-220 (Pb-Free)	50 Units/Rail	
NTB75N03L09	D <sup>2</sup> PAK	50 Units/Rail	
NTB75N03L09G	D <sup>2</sup> PAK (Pb-Free)	50 Units/Rail	
NTB75N03L09T4	D <sup>2</sup> PAK	800 Tape & Reel	
NTB75N03L09T4G	D <sup>2</sup> PAK (Pb-Free)	800 Tape & Reel	

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## **ELECTRICAL CHARACTERISTICS** ( $T_A = 25^{\circ}C$ unless otherwise noted)

	Symbol	Min	Тур	Max	Unit	
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (Note 2) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 µAdc) Temperature Coefficient (Negative)			30	34 –57	- -	Vdc mV°C
Zero Gate Voltage Drain Current $(V_{DS} = 30 \text{ Vdc}, V_{GS} = 0 \text{ Vdc})$ $(V_{DS} = 30 \text{ Vdc}, V_{GS} = 0 \text{ Vdc}, T_J = 150^{\circ}\text{C})$			- -	_ _	1.0 10	μAdc
Gate-Body Leakage Current	$(V_{GS} = \pm 20 \text{ Vdc}, V_{DS} = 0 \text{ Vdc})$	I <sub>GSS</sub>	-	-	±100	nAdc
ON CHARACTERISTICS (Note	2)		•	•	-	
Gate Threshold Voltage (Note 2) $ (V_{DS} = V_{GS}, I_D = 250 \ \mu Adc) $ Threshold Temperature Coefficient (Negative)			1.0	1.6 -6	2.0	Vdc mV°C
Static Drain-to-Source On-Resistance (Note 2) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 37.5 Adc)			-	6.5	8.0	mΩ
Static Drain-to-Source On Resistance (Note 2) ( $V_{GS} = 10 \text{ Vdc}$ , $I_D = 75 \text{ Adc}$ ) ( $V_{GS} = 10 \text{ Vdc}$ , $I_D = 37.5 \text{ Adc}$ , $T_J = 125^{\circ}\text{C}$ )			- -	0.52 0.35	0.68 0.50	Vdc
Forward Transconductance (Notes 2 & 4) (V <sub>DS</sub> = 3 Vdc, I <sub>D</sub> = 20 Adc)			_	58	_	mΩ
DYNAMIC CHARACTERISTICS	6 (Note 4)					
Input Capacitance	// 25 \/d= // 0	C <sub>iss</sub>	-	4398	5635	pF
Output Capacitance	$(V_{DS} = 25 \text{ Vdc}, V_{GS} = 0, f = 1.0 \text{ MHz})$	C <sub>oss</sub>	-	1160	1894	
Transfer Capacitance		C <sub>rss</sub>	-	317	430	
SWITCHING CHARACTERISTI	<b>CS</b> (Notes 3 & 4)					
Turn-On Delay Time	()/ E 0.\/de	t <sub>d(on)</sub>	_	16	30	ns
Rise Time	$(V_{GS} = 5.0 \text{ Vdc}, V_{DD} = 20 \text{ Vdc}, I_{D} = 75 \text{ Adc},$	t <sub>r</sub>	_	130	200	
Turn-Off Delay Time	$R_G = 4.7 \Omega$ ) (Note 2)	t <sub>d(off)</sub>	_	65	110	
Fall Time		t <sub>f</sub>	_	105	175	
Gate Charge	$(V_{GS} = 5.0 \text{ Vdc}, \ I_D = 75 \text{ Adc}, \ V_{DS} = 24 \text{ Vdc}) \text{ (Note 2)}$	$Q_{T}$	-	57	75	nC
		$Q_1$	_	11	15	
		$Q_2$	_	34	50	
SOURCE-DRAIN DIODE CHAP	RACTERISTICS					
Forward On–Voltage	$(I_S = 75 \text{ Adc}, V_{GS} = 0 \text{ Vdc})$ $(I_S = 75 \text{ Adc}, V_{GS} = 0 \text{ Vdc}, T_J = 125^{\circ}\text{C})$ (Note 2)	V <sub>SD</sub>	-	1.19 1.09	1.25 -	Vdc
Reverse Recovery Time	/ Time $ (I_S = 75 \text{ Adc}, V_{GS} = 0 \text{ Vdc} \\  d _S/dt = 100 \text{ A/$\mu$s) (Note 2) } $	t <sub>rr</sub>	_	37	-	ns
(Note 4)		t <sub>a</sub>	-	20	-	
Reverse Recovery Stored		t <sub>b</sub>	-	17	-	μC
Charge (Note 4)		$Q_{RR}$	_	0.023	_	

- Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.
   Switching characteristics are independent of operating junction temperatures.
   From characterization test data.

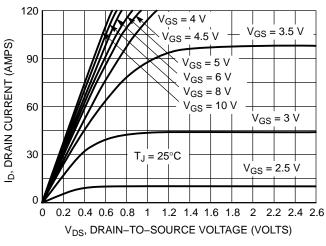


Figure 1. On-Region Characteristics

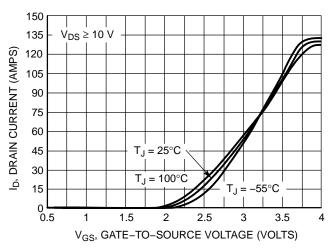


Figure 2. Transfer Characteristics

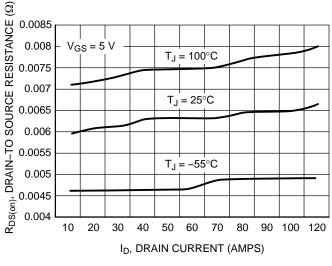


Figure 3. On-Resistance vs. Drain Current and **Temperature** 

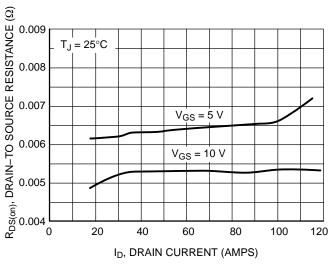


Figure 4. On-Resistance vs. Drain Current and **Gate Voltage** 

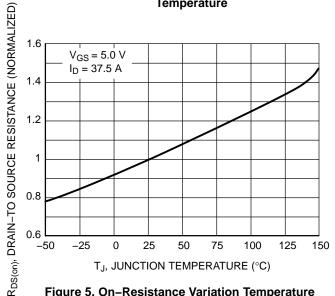


Figure 5. On-Resistance Variation Temperature

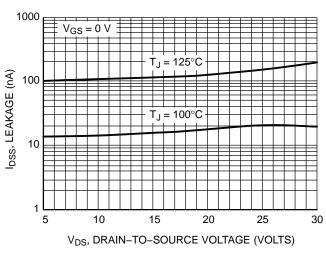


Figure 6. Drain-to-Source Leakage Current vs. Voltage

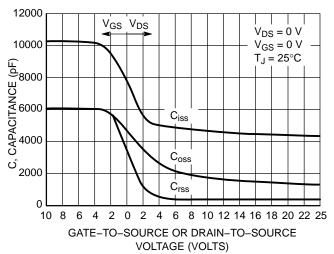


Figure 7. Capacitance Variation

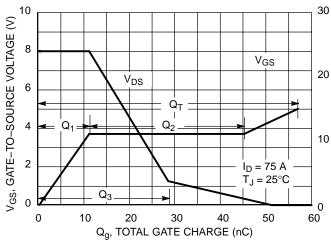


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

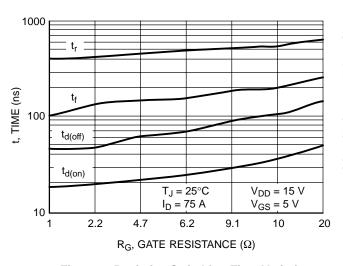


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

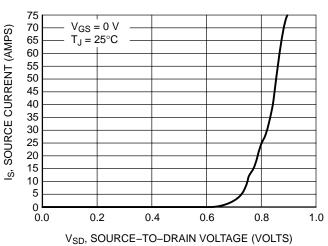


Figure 10. Diode Forward Voltage vs. Current

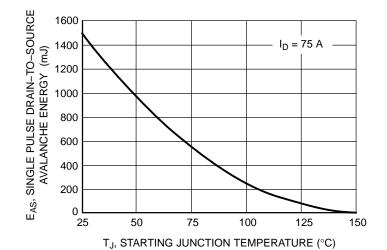
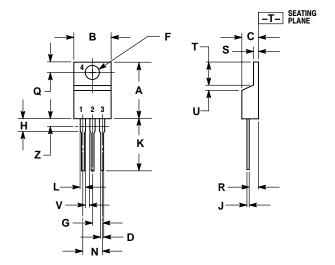


Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature

### **PACKAGE DIMENSIONS**

TO-220 CASE 221A-09 ISSUE AA



- NOTES:
  1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

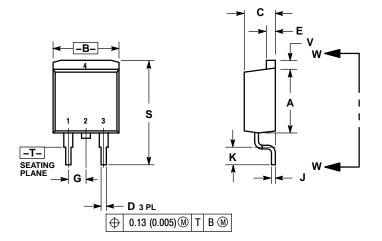
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.570	0.620	14.48	15.75
В	0.380	0.405	9.66	10.28
С	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
Н	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
Т	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
٧	0.045		1.15	
Z		0.080		2.04

- STYLE 5:
  PIN 1. GATE
  2. DRAIN
  3. SOURCE
  4. DRAIN

### **PACKAGE DIMENSIONS**

#### D<sup>2</sup>PAK

CASE 418AA-01 **ISSUE O** 

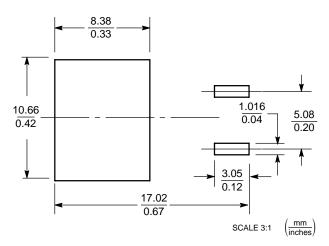


- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH.

	INCHES MILLIMETER		IETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.340	0.380	8.64	9.65
В	0.380	0.405	9.65	10.29
С	0.160	0.190	4.06	4.83
D	0.020	0.036	0.51	0.92
E	0.045	0.055	1.14	1.40
F	0.310		7.87	
G	0.100 BSC		2.54 BSC	
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
M	0.280		7.11	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1 14	1 40

- STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN

#### **SOLDERING FOOTPRINT\***



\*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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