NTP75N03L09, NTB75N03L09

Power MOSFET 75 Amps, 30 Volts

N−Channel TO−220 and D^{2}PAK

This Logic Level Vertical Power MOSFET is a general purpose part that provides the “best of design” available today in a low cost power package. Avalanche energy issues make this part an ideal design in. The drain−to−source diode has a ideal fast but soft recovery.

Features

- Ultra−Low $R_{DS(on)}$, Single Base, Advanced Technology
- SPICE Parameters Available
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperatures
- High Avalanche Energy Specified
- ESD JEDAC Rated HBM Class 1, MM Class B, CDM Class 0
- Pb−Free Packages are Available

Typical Applications

- Power Supplies
- Inductive Loads
- PWM Motor Controls
- Replaces MTP75N03HDL and MTB75N03HDL in Many Applications

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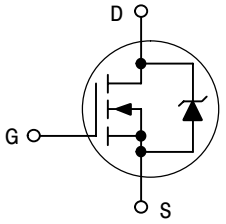
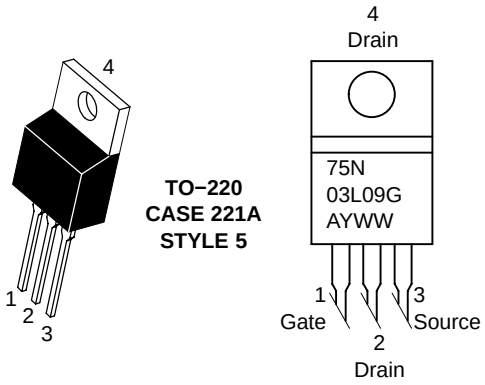
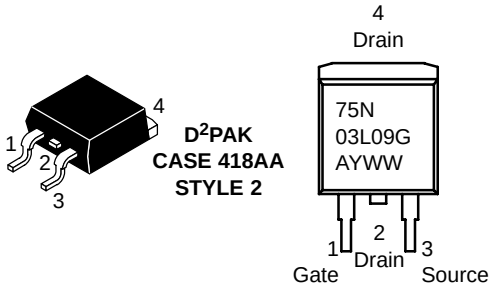
75 AMPERES, 30 VOLTS
$R_{DS(on)}$ = 8 mΩ

N−Channel



MARKING DIAGRAMS & PIN ASSIGNMENTS





75N03L09	= Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	30	Vdc
Drain−to−Gate Voltage (RGS = 10 MΩ)	V_{DGB}	30	Vdc
Gate−to−Source Voltage − Continuous	V_{GS}	±20	Vdc
Non−repetitive (tp ≤ 10 ms)	V_{GS}	±24	Vdc
Drain Current − Continuous @ T_C = 25°C − Continuous @ T_C = 100°C − Single Pulse (tp ≤ 10 μs)	 I_D I_D I_{DM}	 75 59 225	 Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (Note 1)	P_D	125 1.0 2.5	W W/°C W
Operating and Storage Temperature Range	T_J and T_{stg}	−55 to 150	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 38 Vdc, V_{GS} = 10 Vdc, L = 1 mH, I_L(pk) = 55 A, V_{DS} = 40 Vdc)	E_{AS}	1500	mJ
Thermal Resistance − Junction−to−Case − Junction−to−Ambient − Junction−to−Ambient (Note 1)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 1.0 62.5 50	 °C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using the minimum recommended pad size.

ORDERING INFORMATION

Device	Package	Shipping†
NTP75N03L09	TO−220	50 Units/Rail
NTP75N03L09G	TO−220 (Pb−Free)	50 Units/Rail
NTB75N03L09	D^2PAK	50 Units/Rail
NTB75N03L09G	D^2PAK (Pb−Free)	50 Units/Rail
NTB75N03L09T4	D^2PAK	800 Tape & Reel
NTB75N03L09T4G	D^2PAK (Pb−Free)	800 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−Source Breakdown Voltage (Note 2) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{(BR)DSS}$	30	34 −57	− −	Vdc mV°C
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	− −	− −	1.0 10	μAdc
Gate−Body Leakage Current	(V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	−	−	±100	nAdc
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage (Note 2) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	1.0 −	1.6 −6	2.0 −	Vdc mV°C
Static Drain−to−Source On−Resistance (Note 2) (V_{GS} = 5.0 Vdc, I_D = 37.5 Adc)		$R_{DS(on)}$	−	6.5	8.0	mΩ
Static Drain−to−Source On Resistance (Note 2) (V_{GS} = 10 Vdc, I_D = 75 Adc) (V_{GS} = 10 Vdc, I_D = 37.5 Adc, T_J = 125°C)		$V_{DS(on)}$	− −	0.52 0.35	0.68 0.50	Vdc
Forward Transconductance (Notes 2 & 4)	(V_{DS} = 3 Vdc, I_D = 20 Adc)	g_{FS}	−	58	−	mΩ
DYNAMIC CHARACTERISTICS (Note 4)						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	−	4398	5635	pF
Output Capacitance		C_{oss}	−	1160	1894	
Transfer Capacitance		C_{rss}	−	317	430	
SWITCHING CHARACTERISTICS (Notes 3 & 4)						
Turn−On Delay Time	(V_{GS} = 5.0 Vdc, V_{DD} = 20 Vdc, I_D = 75 Adc, R_G = 4.7 Ω) (Note 2)	$t_{d(on)}$	−	16	30	ns
Rise Time		t_r	−	130	200	
Turn−Off Delay Time		$t_{d(off)}$	−	65	110	
Fall Time		t_f	−	105	175	
Gate Charge	(V_{GS} = 5.0 Vdc, I_D = 75 Adc, V_{DS} = 24 Vdc) (Note 2)	Q_T	−	57	75	nC
		Q_1	−	11	15	
		Q_2	−	34	50	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 75 Adc, V_{GS} = 0 Vdc) (I_S = 75 Adc, V_{GS} = 0 Vdc, T_J = 125°C) (Note 2)	V_{SD}	− −	1.19 1.09	1.25 −	Vdc
Reverse Recovery Time (Note 4)	(I_S = 75 Adc, V_{GS} = 0 Vdc dI_S/dt = 100 A/μs) (Note 2)	t_{rr}	−	37	−	ns
		t_a	−	20	−	
Reverse Recovery Stored Charge (Note 4)		t_b	−	17	−	μC
		Q_{RR}	−	0.023	−	

2. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.
4. From characterization test data.

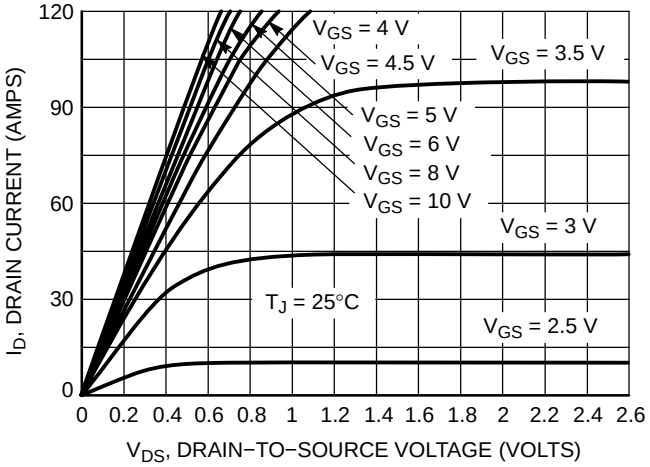


Figure 1. On−Region Characteristics

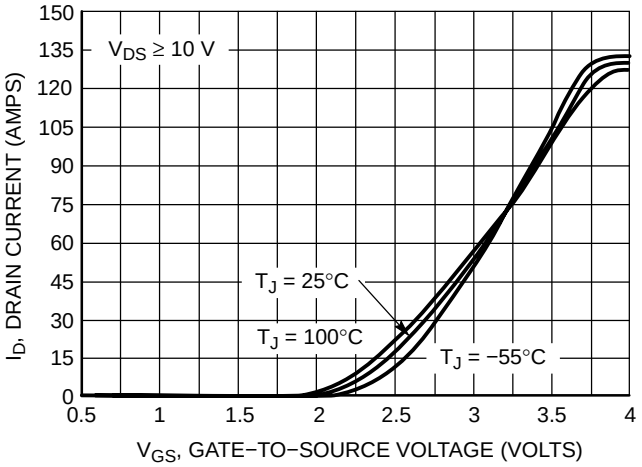


Figure 2. Transfer Characteristics

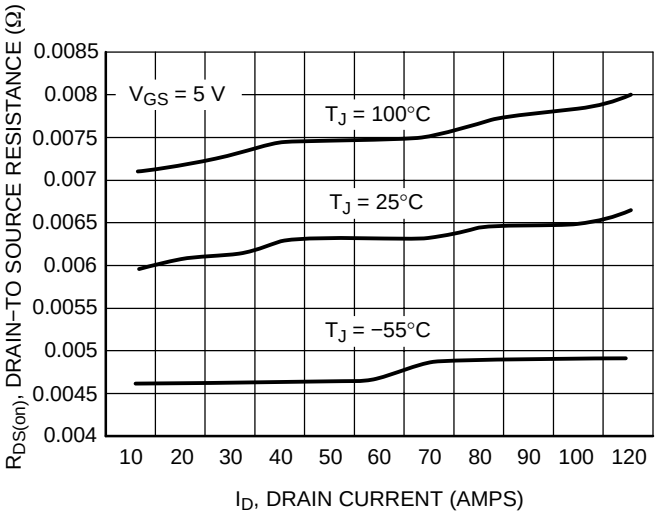


Figure 3. On−Resistance vs. Drain Current and Temperature

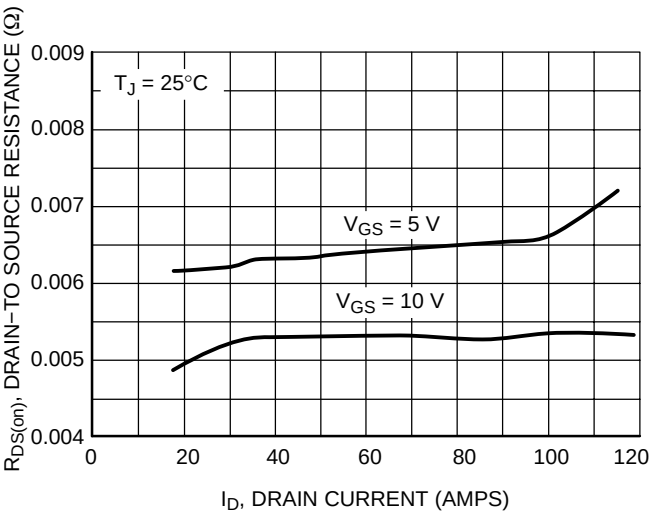


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

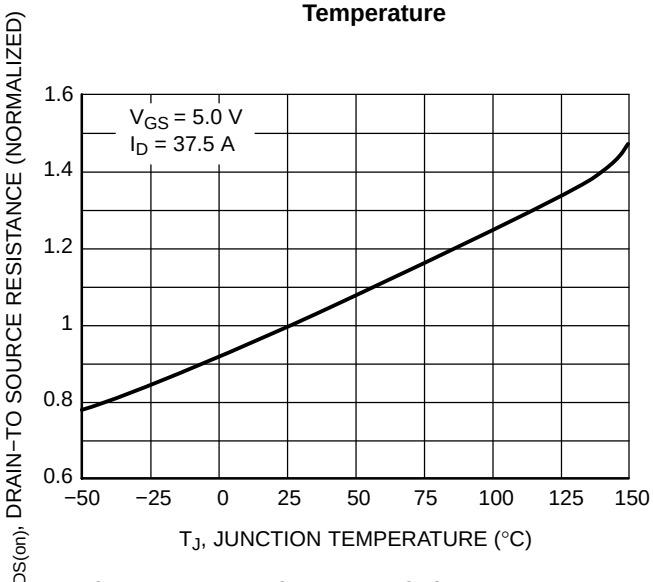


Figure 5. On−Resistance Variation Temperature

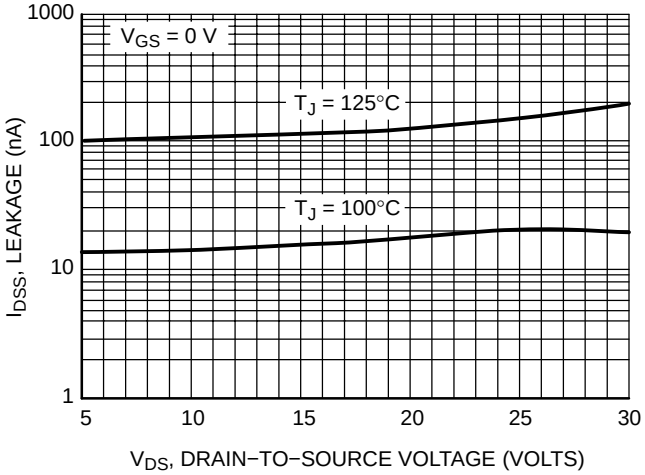


Figure 6. Drain−to−Source Leakage Current vs. Voltage

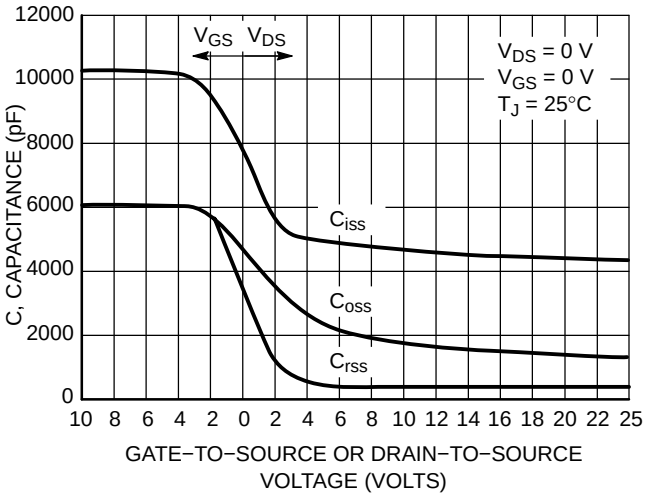


Figure 7. Capacitance Variation

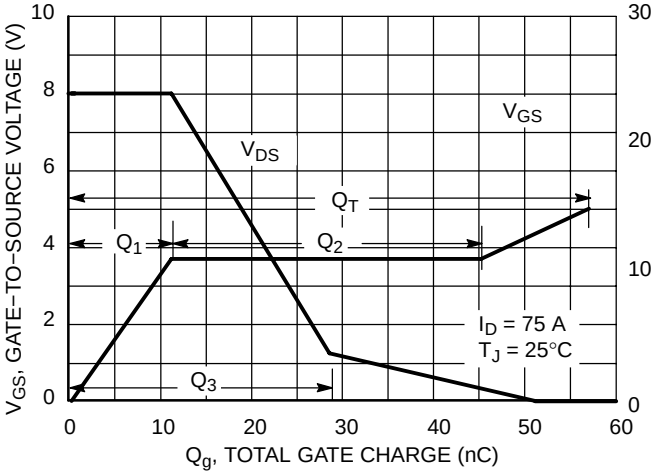


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

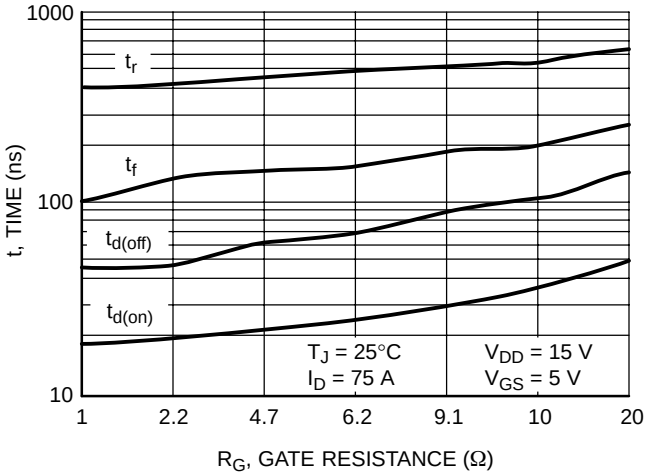


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

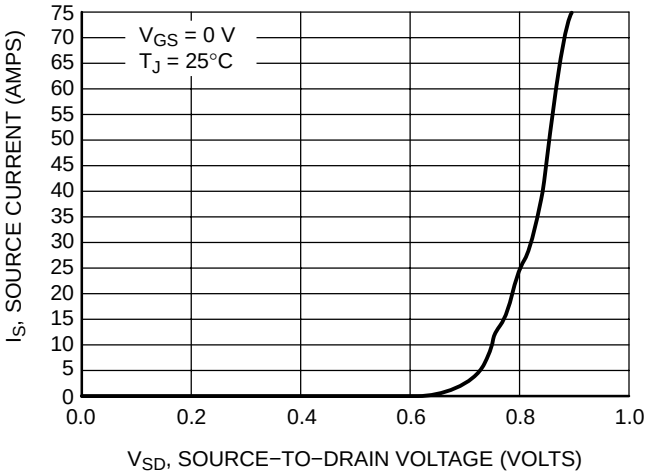


Figure 10. Diode Forward Voltage vs. Current

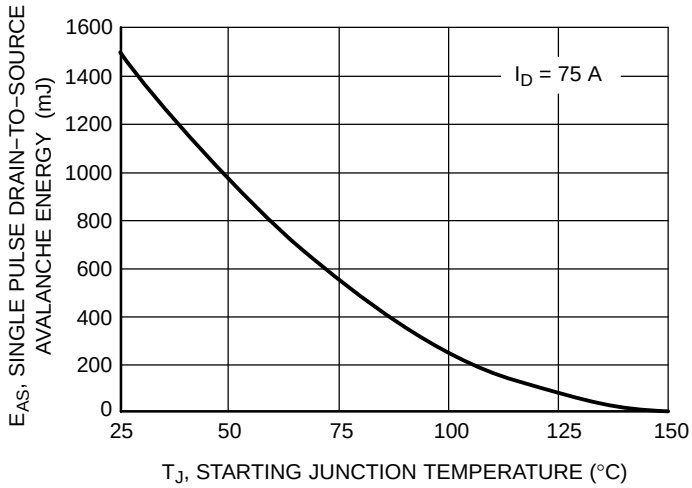
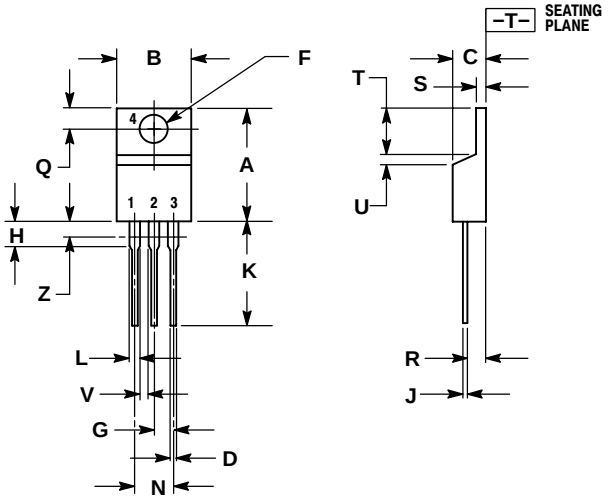


Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AA



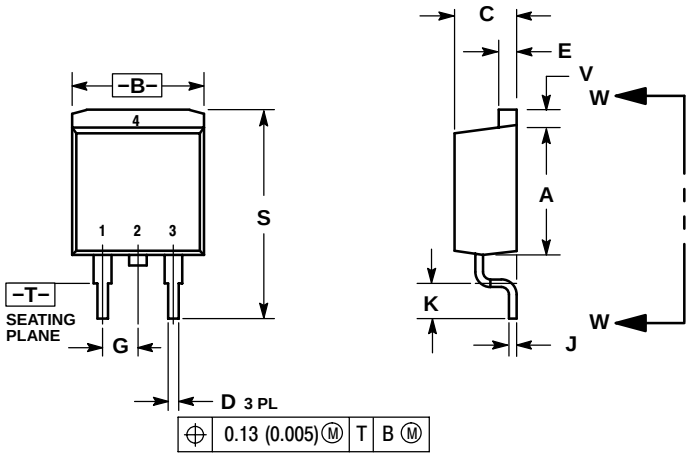
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PACKAGE DIMENSIONS

D²PAK
CASE 418AA−01
ISSUE O

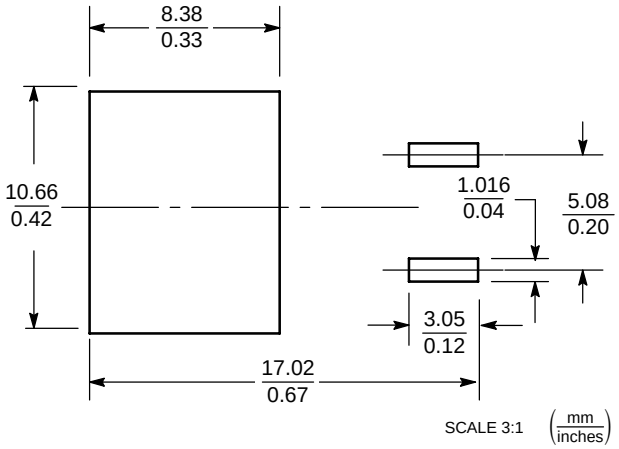


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.036	0.51	0.92
E	0.045	0.055	1.14	1.40
F	0.310	−−−	7.87	−−−
G	0.100 BSC		2.54 BSC	
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
M	0.280	−−−	7.11	−−−
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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